



IN THE  
UNITED STATES PATENT AND TRADEMARK OFFICE

Inventor(s): Padmanabha VENKITAKRISHNAN, et al.

Confirmation No.: 8711

Application No.: 09/916,598

Examiner: Knoll, C. H.

Filing Date: 07/26/01

Group Art Unit: 2112

Title: A CACHE COHERENT SPLIT TRANSACTION MEMORY BUS ARCHITECTURE AND  
PROTOCOL FOR A MULTI PROCESSOR CHIP DEVICE

Commissioner for Patents  
PO Box 1450  
Alexandria, VA 22313-1450

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Technology Center 2100

PETITION FOR EXTENSION OF TIME

Sir:

In an Office Action mailed on 01/07/04, on the above-identified U.S. Patent application, a shortened statutory period of 3 months was set for response. In accordance with 37 C.F.R. 1.136(a), applicant(s) hereby request(s) a:

- ☒ one month
- ☐ two months
- ☐ three months
- ☐ four months

time extension so that the period for response to the Office Action expires on 05/07/04. Authorization to charge the fee required by 37 CFR 1.17 to Deposit Account 23-0085 appears in the enclosed transmittal letter. At any time during the pendency of this application, please charge any fees required or credit any over payment to Deposit Account 08-2025 pursuant to 37 CFR 1.25. Additionally please charge any fees to Deposit Account 08-2025 under 37 CFR 1.16 through 1.21 inclusive, and any other sections in Title 37 of the Code of Federal Regulations that may regulate fees. A duplicate copy of this sheet is enclosed.

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Signature: Desiree Caldwell

Respectfully submitted,

**Padmanabha VENKITAKRISHNAN, et**

By John P. Wagner, Jr.

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Reg. No. **35,398**

Date: 05/07/04

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